Remarks

In view of the above amendments and the following remarks, reconsideration and further examination are requested.

The specification and abstract have been reviewed and revised to make a number of editorial revisions. A substitute specification and abstract have been prepared and are submitted herewith. No new matter has been added.

Claims 6-11 have been cancelled without prejudice or disclaimer to the subject matter contained therein. New claims 12 and 13 have been added.

Claims 1-3 and 5 have been rejected under 35 U.S.C. §102(b) as being anticipated by Kondo (US 6,392,265). Claims 1, 2, 4 and 5 have been rejected under 35 U.S.C. §102(b) as being anticipated by Bailey (US 6,249,014).

Claim 1 has been amended so as to further distinguish the present invention from the references relied upon in the above-mentioned rejections.

In addition, claims 1-3 and 5 have been amended to make a number of editorial revisions. These revisions have been made to place the claims in better U.S. form. None of these amendments have been made to narrow the scope of protection of the claims, nor to address issues related to patentability and therefore, these amendments should not be construed as limiting the scope of equivalents of the claimed features offered by the Doctrine of Equivalents.

The above-mentioned rejections are submitted to be inapplicable to the amended claims for the following reasons.

Claim 1 is patentable over Kondo and Bailey, since claim 1 recites a semiconductor device having, in part, an interlayer insulating layer formed on a substrate, the interlayer insulating layer having a contact hole, a ferroelectric capacitor, and an insulating side wall film covering a peripheral section of the ferroelectric capacitor electrically insulating the peripheral section of the ferroelectric capacitor from a wiring layer, and being spaced from a peripheral edge section of the contact hole. Kondo and Bailey both fail to disclose or suggest the insulating side wall film as recited in claim 1.

Kondo discloses a semiconductor device includes an interlayer isolation film 22 located on a silicon substrate 10 having a drain/source layer 20. The interlayer isolation film 22 has a contact hole 23 therein. The semiconductor device also has a capacitor 70

with a ferroelectric film 66 contained therein. A silicon oxide film 50 covers the sides and most of the top of the capacitor 70, except for a contact hole 52, and also covers the majority of the surface of the semiconductor device on which the capacitor 70 is mounted. An interconnection 56 is formed on the silicon oxide film 50 and connects the top of the capacitor 70 to the drain/source layer 20 by way of the contact holes 23 and 52. (See column 6, line 51 – column 7, line 14 and Figure 8A).

In the rejection of claim 1, it is indicated that the silicon oxide film 50 corresponds to the claimed insulating side wall film and the contact hole 23 corresponds to the claimed contact hole. However, it is noted that the claimed insulating side wall film is recited as being spaced from a peripheral edge section of the contact hole. As can be clearly seen from Figure 8A of Kondo, the silicon oxide film 50 completely surrounds the contact hole 23 and is not spaced from a peripheral edge section of the contact hole 23. As a result, it is apparent that Kondo fails to disclose or suggest the present invention as recited in claim 1.

Bailey discloses a memory cell 1070 having a ferroelectric capacitor 1072 and an access transistor 100. The ferroelectric capacitor 1072 has an underlying barrier material 1074 on its bottom surface and a hydrogen barrier material 1086 located on its sides and a majority of its top surface. A metallization layer 1092 connects the top surface of the ferroelectric capacitor 1072 to the transistor 100 by way of a contact hole in the hydrogen barrier material 1086 and a contact hole to the right of the ferroelectric capacitor 1072. (See column 11, lines 28-59 and Figure 9B).

In the rejection of claim 1, it is indicated that hydrogen barrier material 1086 corresponds to the claimed insulating side wall film, the contact hole to the right of the ferroelectric capacitor 1072 corresponds to the claimed contact hole, and the metallization layer 1092 corresponds to the claimed wiring layer. However, it is noted that the claimed insulating side wall film is recited as being spaced from a peripheral edge section of the contact hole. As can be seen from Figure 9B of Kondo, the hydrogen barrier material 1086 is not illustrated as being spaced from a peripheral edge section of the contact hole to the right of the ferroelectric capacitor 1072.

Further, the claimed insulating side wall film covering a peripheral section of the ferroelectric capacitor is recited as electrically insulating the peripheral section of the

ferroelectric capacitor from the wiring layer. Again, Figure 9B of Bailey illustrates that the hydrogen barrier material 1086 does not insulate the peripheral section of the ferroelectric capacitor 1072 from the metallization layer 1092. Instead, there appears to be another material (see element 118 in Figure 5 of Bailey) insulating the ferroelectric capacitor 1072 from the metallization layer 1092. As a result, it is apparent that Bailey also fails to disclose or suggest the present invention as recited in claim 1.

Because of the above-mentioned distinctions, it is believed clear that claims 1-5, 12 and 13 are allowable over the references relied upon in the rejections. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time of invention would not have been motivated to make any combination of the references of record in such a manner as to result in, or otherwise render obvious, the present invention as recited in claims 1-5, 12 and 13. Therefore, it is submitted that claims 1-5, 12 and 13 are clearly allowable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. The Examiner is invited to contact the undersigned by telephone if it is felt that there are issues remaining which must be resolved before allowance of the application.

Respectfully submitted,

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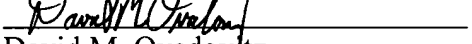
By: 

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